WHAT IS CLAIMED IS:

1. An integrated circuit comprising:
a plurality of pins; and
at least one scan path per pin.

2. The integrated circuit of claim 1 wherein:
a first I/O pin is operable to input scan test data at a first test time; and
the first I/O pin is operable to output scan test data at a second test time.

3. The integrated circuit of claim 2 wherein:
the first I/O pin is operable to input scan test data to a first scan path at the first test time;
a second I/O pin is operable to input scan test data to a second scan path at the first test time;
the first I/O pin is operable to output scan test data from the second scan path at the second test time; and
the second I/O pin is operable to output scan test data from the first scan path at the second test time.

4. The integrated circuit of claim 3 wherein the first scan path further comprises a series of scan paths.

5. The integrated circuit of claim 2 further comprising a series of scan paths wherein:
the first I/O pin is operable to input scan test data to the series at a first test time; and
the first I/O pin is operable to output scan test data from the series at a second test time.

6. The integrated circuit of claim 2 further comprising functional circuitry wherein:
the scan path interacts with the functional circuitry; and
the I/O pin is operable to input scan test data at the first test time; and
the I/O pin is operable to output scan test data at the second test time.

7. The integrated circuit of claim 2 further comprising functional circuitry wherein:

the I/O pin is operable to input functional test data at the first test time; and

the I/O pin is operable to output functional test data at a the second test time.

8. An integrated circuit comprising:

a first I/O pin operable to receive input data during a test time; and

a second I/O pin operable to provide output data during the test time.

9. The integrated circuit of claim 8 further comprising a first scan path wherein:

the first I/O pin is operable to input scan test data during the test time; and

the second I/O pin is operable to output scan test data during the test time.

10. The integrated circuit of claim 9 further comprising a second scan path wherein:

the first I/O pin is operable to input scan test data to the first scan path during the test time;

the output from the first scan path is input to the second scan path; and

the second I/O pin is operable to output scan test from the second scan path data during the test time.

11. The integrated circuit of claim 9 further comprising any number of scan paths and the same number of I/O pins wherein:

each I/O pin is operable to input scan test data during the test time;

each I/O pin is operable to input scan test data during the test time; and

a tester determines the function of each I/O pin during the test time.

12. An integrated circuit comprising;

a functional circuit operable to produce functional output;

a scan path operable to produce scan output;

an I/O pin operable to be used as input at a first time and as output at a second time; and

a flip-flop coupled to the I/O pin and to the functional circuit and the scan path operable to hold the functional output or the scan output for a clock cycle.

13. The integrated circuit of claim 12 further comprising:
a number of scan paths;
the same number of I/O pads; and
the same number of flip-flops operable to form at least one register.

14. The integrated circuit of claim 13 wherein
each I/O pad further comprises a scan output buffer;
each flip-flop further comprises;
a compact-control signal;
an output-data signal; and
an and-gate operable to eliminate don't-care data; and
the register is operable as a compaction register.

15. The integrated circuit of claim 13 wherein:
each I/O pad further comprises;
a reseed multiplexer operable to receive functional output data and scan input data;
a reseed control signal operable to control the reseed multiplexer; and
the register is operable as a reseed register.

16. The integrated circuit of claim 15 wherein:
each I/O pad further comprises an or-gate operable to receive input from the output of a linear feedback shift register; and
the register is operable as a linear feedback shift register.

17. The integrated circuit of claim 13 further comprising a second number of flip-flops operable to form a compaction register wherein:
the integrated circuit is operable to perform reseeding; and
the integrated circuit is at the same time operable to perform compaction.

18. The integrated circuit of claim 17 wherein the compaction register can be read serially.

19. A method comprising:
inputting scan data to an I/O pin during a first time;
processing the scan data in a scan path to produce scan output data; and

outputting the scan output data to the I/O pin at a second time.

20. The method of claim 19 further comprising:
multiplexing output data and scan output data; and
storing the output data or scan output data in a flip-flop during the first time.

21. The method of claim 20 further comprising:
connecting a number of flip-flops associated with I/O pins; and
forming a register performing a reseed test.

22. The method of claim 21 wherein forming a register further comprises:
sending a compact control signal;
and-gating the compact control signal with the output data;
eliminating don't care data; and
performing compaction.

23. The method of claim 21 wherein forming a register further comprises:
sending a reseed control signal to a reseed multiplexer;
multiplexing functional output data and scan input data; and
performing a reseed test.

24. The method of claim 23 wherein multiplexing further comprises:
receiving gated input from a linear feedback shift register; and
performing a linear feedback shift register reseed test.

25. The method of claim 19 wherein the first time and the second time occur during the same clock cycle.